Temperature Stable Ring Oscillator Based on the Mismatch Compensation of the Biasing Current

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***Abstract*- In this paper, a low temperature coefficient (TC) current reference using the mismatch compensation method is proposed. The temperature independent reference current is generated by scaling the W/L ratio of voltage mirror and adjusting the difference in biasing resistances. The basing current dependent TC and the optimum design strategies for MOSFET and resistors will be discussed in the following. The current reference has been fabricated in CSMC 0.35μm CMOS process. SPICE simulation results show that a minimums TC of the current reference is 5.6ppm/ºC within the range of –40ºC~125ºC, and the output current is about 6μA. The experimental results suffer from a considerable degradation due to practical accuracy control limitation.**

Keywords- Current Reference; Nonlinear Compensate; Temperature Coefficient; Mismatch Control; Ring Oscillator

I. INTRODUCTION

Current and voltage references are indispensable circuit in analog, digital and power electronic systems [1].These should be designed stable as possible, the current and voltage references with high temperature immunity for proper operation. They are usually used to determine biasing points of sensitive analog circuits, such as amplifiers, oscillators, phase-lock loops (PLLs) [2]. Since most of electrical parameters are TVP (temperature, voltage and process) sensitive, thus the TVP stable current reference can make the integrated circuits operate more robustness in achieving high circuit performance.

For simplifying the circuit structure and improving the operation frequency, the ring oscillator and the variant types are widely used as clock generation circuit. In order to improve the stability of the oscillation frequency, the constant current or even current reference is introduced in the circuit during charge or discharge timing control [3]. The maximum dynamic power consumption of the digital circuits driven under the clock with frequency f given above, can be temperature-stable as

$$P_{dynamic} = \alpha \times C \times V_{dd}^2 \times f \quad (1)$$

Where α is the activity factor which reflects the possibility of the circuit operation under the dynamic procedure, C is the total equivalent load capacitance, V_{dd} is the supply voltage. Since the classical PTAT (proportional to absolute temperature) biasing current with positive TC (temperature coefficient) is adopted in most situations, thus the operation frequency f is varied obviously with the temperature. The dynamic power consumption for digital circuits as well as static power consumption for analog circuit are increased nearly 50% from low temperature of -55ºC to room temperature, or from room temperature to high temperature of 125ºC respectively. The power consumption of the circuits will almost be doubled when the temperature varied from -55ºC to 125ºC, and for this reason the current efficiency of the circuit is seriously deteriorated.

In order to restrict the energy consumption under wide dynamic temperature range, or sustain high temperature immunity for proper operation, many high precision, temperature-stable voltage and current reference circuits have been proposed and developed in CMOS technology process over the last decades [4, 5]. However, as mentioned before, the conventional self-biased current circuit either by V/R or ΔV/R [6], can hardly be designed to meet the requirement due to the temperature sensitivity of the applied voltage and the resistance.

The present widely used temperature compensation principle in current reference is similar with that in bandgap voltage reference [7]. That is to say, the approximately PTAT current with its positive temperature coefficient (TC) is mixed with the negative TC current deriving from V_{GS} or V_{BE} to generate nearly zero TC current. The output current generated by direct current summing, or by V-I transfer circuit which consisted of high gain low offset operation amplifier, can be both used in generating the current reference.

Since the current as mentioned above are both defined by the resistors, so that the TC of current reference (CR) is closely related with the resistance selected [8]. As mentioned above, it is more difficult to obtain temperature stable current reference than that of voltage reference. Till now, the practical TC of current references implemented by different compensation sachems are still in the range of several tens or more of ppm/°C [9-12], which is at least an order or more of magnitude larger than that of voltage reference.

Except the complicated structure and degradation in power supply rejection ratio, the primary problem within the present CR is temperature performance degradation under the CMOS process variation due to existed random or systematic mismatch errors [13-15]. However, if the mismatch can be well controlled within a wide temperature range, an accurate and process robustness current reference can be obtained in a simple way by this new kind of mismatch based compensation strategy.

The remaining contents in this paper are organized as follows. In Section 2, the temperature model of modified compensation is presented. In Section 3, a mismatch based temperature compensation principle is described. Circuit design and application as well as helpful discussions are presented and summarized in Section 4. The error analysis and reduction methods are discussed in Section 5, followed by conclusions in Section 6.

II. THE TEMPERATURE MODEL OF MODIFIED COMPENSATION

As widely used in BGR, the turn on voltage of V_{BE} has a stable negative TC of around -2mV/ºC, and the differential voltage between two different size diodes under the same current biasing can be given as $\Delta V_{EB}=V_T \ln N$, where N is the fixed ratio of two diodes emitter area, and the thermal or PTAT voltage, $V_T=kT/q$, has a constant positive TC of +0.087mV/ºC, nearly 1/23 of that of the negative TC due to the electron charge q and the Boltzmann constant k both are constant. And T is the absolute temperature, so V_T is nearly 26mV at room temperature. Driven by self-biased circuit, $\Delta V_{BE}/R_0$ and V_{BE}/R_1 are summed at the output branch to form an output current as

$$I_o = \frac{V_{BE}}{R_1} + \frac{\Delta V_{BE}}{R_0} = \frac{1}{R_1}(V_{BE} + \frac{R_1}{R_0} V_T \ln N) = \frac{V_{eff}}{R_1} \quad (2)$$

Where $V_{eff}=V_{BE}+mV_T$, the linear coefficient $m=(R_1/R_0)\ln N$ is used in temperature compensation for the effective voltage V_{eff}. In order to obtain the zero TC of V_{eff}, m≈23 is needed. However, in order to obtain the minimum residual TC in CR, it requires that V_{eff} must be completely matched with biasing resistor in a wide temperature range. Unfortunately, almost all the crucial parameters such as resistance, mobility and turn-on voltage of V_{BE} or V_{GS} all vary with temperature nonlinearly, so that the compensation of the output current requires configurable TC of V_{eff} and R_1.

The proposed temperature compensation for CR is completely different from the ordinary method by mixing two kinds of current with opposite TC. The new compensation strategy is using ΔV_{BE} and ΔV_{GS} concurrently by artificial devices variation in size or dimensions.

Fig. 1 presents a modified three branches of circuit for current reference generation, where the PMOS linear current mirror is used to defined $I_1=I_2$ for two core branches, and the ratio of emitter area for Q_0 and Q_1 is set as N: 1 with N>1, at the same time the W/L relationship for M1 and M0 is set as M: 1 with M>1.In this way the different potentials at the source of M_0 and M_1 bring a mismatch voltage of ΔV_{GS} due to $V_X \neq V_Y$. An additional resistor of R_1 in Q_1/M_1 branch is added to obtain $\Delta R=R_0-R_1$ for temperature compensation.

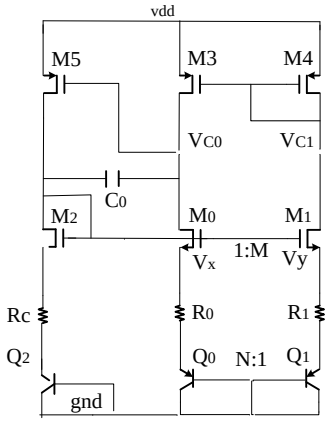


Fig.1 Compact temperature compensation for current reference

The basic constraint by the circuit is given as $V_{GS0}+I_{0R0}+V_{BE0}=V_{GS1}+I_{1R1}+V_{BE1}$. If the differential voltage and resistance are defined as $\Delta V_{GS}=V_{GS0}-V_{GS1}$, $\Delta V_{BE}=V_{BE1}-V_{BE0}$ and $\Delta R=R_1-R_0$, and the well matched current $I_0=I_1=I_{DS}$ is achieved, the generated current by two coupling of nonlinear current mirrors can be rewritten in the new form as:

$$I_1 = \frac{(V_{GS0}-V_{GS1})-(V_{BE1}-V_{BE0})}{R_0-R_1} = \frac{\Delta V_{GS}-\Delta V_{BE}}{\Delta R} = \frac{\Delta V_{eff}}{\Delta R} \quad (3)$$

As shown in fig.1, the relative larger size of BJT and NMOS should be located on the diagonal position, and $\Delta V_{GS}>0$ when M>1, $\Delta V_{BE}>0$ when N>1. Clearly, the current given above can be reduced to traditional PTAT biasing of $I_1=\Delta V_{BE}/R$ when $\Delta V_{GS}=0$ by M=1 and $R_2=0$. If ΔV_{BE} and ΔV_{GS} are linearly related, the generated current will also have PTAT feature; If ΔV_{BE} and ΔV_{GS} are nonlinearly related with the same polarity in TC, the TC of ΔV_{BE}-ΔV_{GS} can be configured closely to that of resistors used in the circuit. In this way the CR can be obtained.

The temperature characteristics of ΔV_{GS} and resistance are clearly discussed below. If the basing currents under strong inversion region are matched well to give $I_0=I_1=I$, thus the ΔV_{GS} can be given by

$$\Delta V_{GS} = \sqrt{\frac{2I_0}{k_0}} - \sqrt{\frac{2I_1}{k_1}} \approx \sqrt{\frac{2I_0}{k_0}}(1-\frac{1}{\sqrt{M}}) \quad (4)$$

Where M is the W/L scaling ratio between two transistors of M_1 and M_0, $k_0=\mu_n C_{ox}(W/L)$ is the gain factor of M_0, and the temperature model for carrier mobility is $\mu_n(T)=\mu_n(T_0)(T/T_0)^{-n}$, the temperature index n is located at a range of $0<n<2$, which is related with the substrate doping concentrate. So the TC of k_0 can be approximately written by

$$\frac{\partial k_0}{\partial T} \approx -n\mu(T_0)(\frac{T}{T_0})^{-n-1}\frac{1}{T_0}C_{ox}(\frac{W}{L})_0 = -nk_0\frac{1}{T} \quad (5)$$

Clearly, the TC is negative for k_0 due to the mobility temperature behaviour, thus the TC is usually positive for ΔV_{GS}, which is

$$\frac{\partial \Delta V_{GS}}{\partial T} \approx \frac{1}{2}(\frac{n}{T}+\frac{1}{I_0}\frac{\partial I_0}{\partial T})\Delta V_{GS} \quad (6)$$

The nonlinear temperature characteristic of ΔV_{GS} under the strong inversion is obviously different with that of ΔV_{BE}, however their positive TC can also be counteracted partially for each other to match with the nonlinear TC of resistance. In SPICE simulation, the nonlinear temperature model for the resistor is given by

$$R_{eff} = R_{eff}(T_0)[1+TC_1\Delta T + TC_2(\Delta T)^2] \quad (7)$$

Where TC_1 and TC_2 are the first and the second order temperature coefficient, $\Delta T=T-T_0$, and R_{eff} can be used to indicate either R, the physical resistance, or ΔR, the differential of two resistances in the same type. Clearly, the temperature variation polarity for ΔR can be freely configured. If ΔR>0, the TC polarity for R and ΔR is the same, otherwise if ΔR<0, an opposite TC polarity for R and ΔR is achieved. Therefore, ΔR with controllable TC polarity can provide considerable freedom in temperature compensation.

III. MISMATCH BASED COMPENSATION METHOD

In conventional basing circuit, the resistor is often used in current definition, however in the proposed circuit, the current definition is changed to the restriction of $\Delta V_{BE}=\Delta V_{GS}$ when ΔR=0. If M_0 and M_1 are both in strong inversion biased with substrate biasing effect ignored, the generated current can be given by

$$I_0 \approx \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_0(\frac{\sqrt{M}}{\sqrt{M}-1}V_T \ln N)^2 = \frac{1}{2}k_0\Delta_{eff}^2 \quad (8)$$

Where, the effective overdrive voltage Δ_{eff} of M_0 belongs to a PTAT voltage. By taking $\mu_n(T)$ into consideration, the temperature property of biasing current is proportional to T^{2-n}, with $n<2$, so that the TC of biasing current is positive. Therefore in this simple situation, the zero TC CR can hardly obtain without using resistance or differential resistance.

In order to obtain the current with low TC, the differential resistance of ΔR is used in current definition, where the basic constraint condition is given by

$$\sqrt{\frac{2I_0}{k_0}}(1-\frac{1}{\sqrt{M}}) = V_T \ln N + I_1\Delta R \quad (9)$$

Taking partial derivative of above equation with respect to T, and applying the result of $\partial I_1/\partial T \approx 0$, the corresponding control condition becomes

$$\frac{n}{T_0^{\frac{n}{2}}}\sqrt{\frac{1}{2\mu_0(T_0)C_{ox}(\frac{W}{L})_{M0}}}(1-\frac{1}{\sqrt{M}})\sqrt{I_1}T^{\frac{n}{2}-1} = \frac{V_{T0}\ln N}{T_0} + I_1\frac{\partial\Delta R}{\partial T} \quad (10)$$

If all the parameters unrelated with temperature in the left side of above equation are represented by the coefficient α, as given by

$$\alpha = \frac{n}{T_0^{\frac{n}{2}}}\sqrt{\frac{1}{2\mu_0(T_0)C_{ox}(\frac{W}{L})_{M0}}}(1-\frac{1}{\sqrt{M}}) \quad (11)$$

Then the above temperature constraint relation can be simplified to

$$\alpha\sqrt{I_1}T^{\frac{n}{2}-1} - I_1\frac{\partial\Delta R}{\partial T} = \frac{V_{T0}\ln N}{T_0} \quad (12)$$

As can be seen from above equation, since $T>0$, the first term in left side is positive due to $\alpha>0$, and the term on the right side of the equation is also positive, so that the term of $\partial\Delta R/\partial T$ can be used for making the relation given above existed. It's convenient to find a suitable ΔR and I_1 to meet the requirements at a specific temperature range, but it's difficult to satisfy the restriction in wide temperature range. Furthermore, because it is a multi-variables optimal problem, the selection of ΔR and I_1 is not unique.

In order to make the constraint condition hold in wide temperature range, we take partial derivative in both sides of Formula (12) with respect to the temperature variable under the approximation of $\partial I_1/\partial T \approx 0$, so

$$\frac{\partial(\partial\Delta R/\partial T)}{\partial T} = \alpha(\frac{n}{2}-1)\sqrt{I_1}T^{\frac{n}{2}-2} \quad (13)$$

It can be seen that the second order TC of ΔR should be negative. The difference with other compensation methods is that the value of biasing current plays an important role in determining the TC of the generated current.

In SPICE simulation, the nonlinear temperature model for the resistor is given by (7). So the first-order and the second-order derivative of differential resistance are

$$\frac{\partial\Delta R}{\partial T} = \Delta R[TC_1 + TC_2(T-T_0)] \quad (14)$$

$$\frac{\partial(\partial\Delta R/\partial T)}{\partial T} = 2\Delta R \times TC_2 \quad (15)$$

If the high impedance poly-silicon resistance with $TC_1<0$ and $TC_2>0$ is used, $\Delta R<0$ or $R_0>R_1$ is needed for better temperature compensation.

The substrate basing effect is ignored in all the discussions as given above. When ΔV_{GS} is not small enough, the mismatch in substrate basing effect between M_0 and M_1 cannot be neglected. An additional contribution by ΔV_{TN} in ΔV_{GS} should be considered, where $\Delta V_{GS}=(\Delta_{M0}-\Delta_{M1})-\Delta V_{TN}$, and $\Delta V_{TN}=V_{TN1}-V_{TN0}$. The scaled ΔV_{TN} can be calculated and given by

$$p = \frac{\Delta V_{TN}}{\Delta V_{GS}} \approx \frac{\gamma_n}{2\sqrt{2\phi_f + V_{SB,M0}}} \quad (16)$$

Where γ_n is substrate biasing coefficient and φ_f is surface potential. If p is small enough and closed to zero, substrate biasing effect can be ignored totally. Otherwise a serious error will generate in above current model due to ΔV_{TN} existed.

Except ΔV_{TN} effect, the current level also has a significant influence on TC of CR. The selected ΔR should be matched with biasing current in decreasing the current TC. A large common mode resistor as defined by $R_C=(R_0+R_1)/2$ is benefit for increasing $V_{SB,M1}$ and reducing the ratio p.

IV. CIRCUIT DESIGN AND APPLICATION

A. Design Issue

The W/L and the current of the MOSFET designed should be able to guarantee the device operating under the strong inversion condition. The compensation strategy is separated into two steps. Firstly, the rough CR is generated under $\Delta R=0$ restriction, where the initial M and N are preset. Secondly, the ΔR is introduced, and M and ΔR are both modified concurrently for further compensation to get a minimum TC of the CR.

The circuit is designed and implemented by CSMC 0.35μm CMOS process. Based on the principle discussed above, the optimum parameters for the proposed CR is presented in Table 1, where M=1.74, $\Delta R=R_0-R_1=2.9k\Omega$, and the squared resistance is 2kΩ, the minimum emitter area for Q_1 and Q_2 are both 10×10 μm^2, and the emitter area ratio for Q_0:Q_1 is usually fixed at N=8.

TableI MISMATCH CONFIGURATION FOR ΔR, M

$(W/L)_{M0}$	$(W/L)_{M1}$	$(L/W)_{R0}$	$(L/W)_{R1}$
2.3μm/7μm	4.0μm/7μm	35.7μm/(5×4μm)	20μm/(5×12μm)

SPICE simulation results for DC and temperature properties under the power supply voltage of V_{DD}=5V are summarized as following. The minimum operation voltage is around 2.1V. The static current in one of the two self-biased branches is around 1.12μA. The current variation is about 7.5nA when the supply voltage increases from 3V to 5V, and the minimum TC is around 5.6ppm/ºC as shown in Fig. 2. Finally, the performances comparison with other designs is

presented in Table 2, where TCs and TCt are the TC of the circuit obtained by simulation and testing results respectively.

TableII CURRENT REFERENCE CIRCUITS PERFORMANCES

Parameters	This work	Ref. [11]	Ref. [12]	Ref. [2]
CMOS Techonology	0.35μm	0.35μm	0.25μm	0.35μm
Supply voltage(V)	5	3	2.5	3.3
Iref(μA)	1.12	0.0949	15.39	17.0
Temp.(ºC)	-40-125	-20-100	0-120	-20-100
TCs(ppm/ºC)	5.6	N/A	720	280
TCt(ppm/ºC)	600	523	520	N/A

The current reference can be used as static biasing current in analogue circuits for temperature stable operation. A simple ring oscillator consisting of 5 inverters under the constant current driving is presented in Figure 3, where two PIP capacitors in the same size are used to control the frequency and duty cycle. The simulated period time and duty cycle at room temperature are 4μs and 50%, respectively.

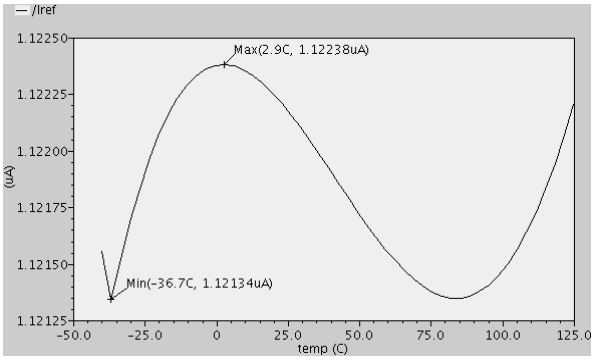


Fig.2 Simulation result of the biasing current

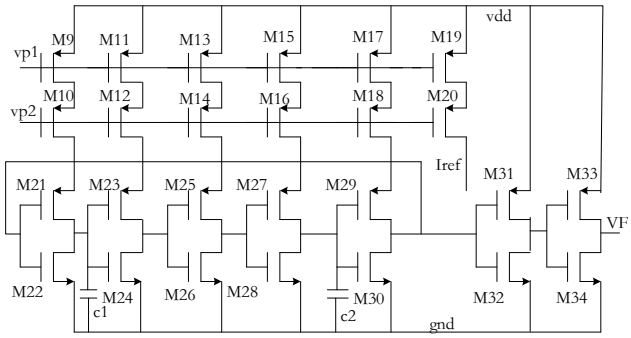
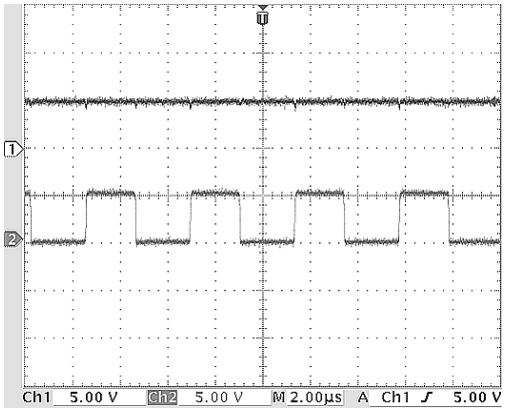


Fig.3 Ring Oscillator driving by current reference

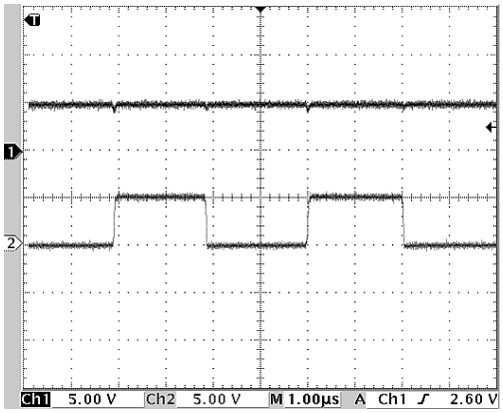
B. *Test Results*

The output CR for biasing the ring oscillator is 10 times of that biasing current of I_0. The tested TC expands more than one order of magnitude of that simulation result. A significant degradation in output current TC mainly comes from the random errors due to unavoidable mismatch of the circuit's structure and the variation of the processor corners. Thus the resistance trimming is necessary, and the size of MOSFETs and resistors should be as large as possible if chip area permits.

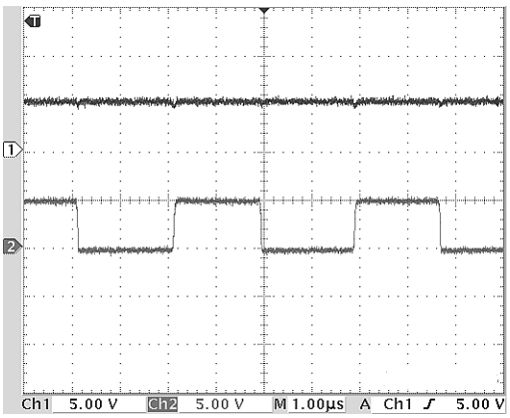
The test results for the clock period of ring oscillator in different temperature are presented in Fig. 4, where the duty cycles are nearly constant with the variational temperature. The tested period times under the three different temperatures of -40ºC, 25ºC and 125ºC are around 4.3μs, 4.1μs and 3.9μs, respectively, giving an average positive TC of 600ppm/ºC for the pulse frequency. It is corresponding to ±5% frequency variation rate within the entire temperature range with respect to the oscillation frequency at room temperature.



(a)



(b)



(c)

Fig. 4 Period time of Ring Oscillator in different temperature

(a) Ts=4.3μs@T=-40º C; (b) Ts=4.1μs@T=25º C; (c) Ts=3.9μs@T=125º C

The capacitance and the critical transition voltage of inverter in oscillator are both temperature sensitive, so the TC of oscillation frequency is different from that of CR. The experimental results show that the TC of output current is sensitive with the mismatch of the circuit, which is either induced artificially by parameter designs or randomly by process fabrication errors. If the suitable resistor trimming structure is used, the influence from process variation and other elements in the circuit can be partially removed. The temperature stability of the circuit performance is improved.

V. THE ERROR ANALYSIS AND REDUCTION METHODS

Although the resistance trimming method is used in the proposed circuit, the restriction between accuracy and dynamic range is still existed. So a brief estimate on the random errors caused by the structure mismatch and the process drift is necessary [16]. A simple analysis of the source of the errors and the possible error diminution principles are summarized and given below.

A. Resistance Process Mismatch and Resistance Tolerance

The absolute deviation for the resistance is far larger than other elements in the circuit, and the practical resistance can be described as $R_{eff}=R(1+\delta_R)$, where R is the designed resistance value and δ_R is resistance tolerance. For differential resistance, the similar result can be obtained as $\Delta R_{eff}=\Delta R(1+\delta_{\Delta R})$. The R_{eff} or ΔR_{eff} is used in the CR circuit, while the resistance ratio is used in BGR circuit. Thus the TC degradation for CR circuit due to resistance errors is more seriously, and the biasing current will be changed a lot. Fortunately, this kind of error can be directly removed by the resistor trimming circuit.

B. Current Mirror Mismatch

The random mismatch between two adjacent transistors caused by device size deviation and threshold voltage deviation will generate a considerable error in the current mirror. It leads to significant TC degradation as compared to the simulation results. Therefore, a large size of devices as well as great power consumption should be adopted to reduce this kind of mismatch. That is to say increasing the channel length L and width W or transistor area S=LW can effectively reduce the deviation caused by process variation. Improving the current or overdrive voltage by small W/L can greatly eliminate the influence of V_{TH} mismatch. Additionally, the symmetrical or balanced layout of the circuit should be used for further mismatch reduction. Clearly, the current mirror mismatch cannot be directly compensated by the resistance trimming technique.

C. Base Area Resistor and β Value Influence

In N-well CMOS process, PNP transistor can only be formed by parasitic vertical structure, where the current gain of β is very low, resulting a large base current I_b. So the voltage drop on the base series resistance r_b will hardly be ignored. In this way the turn on voltage of V_{BE} for PNP transistor is modified as given by

$$V_{\mathrm{BE}} = I_B r_{\mathrm{b}} + V_{\mathrm{T}} \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} = \frac{I_{\mathrm{C}}}{\beta} r_b + V_{\mathrm{T}} \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} \tag{17}$$

Where I_S and I_C are the reversed saturation current of emitter junction and the collector current of PNP parasitic transistor respectively. So under the same current biasing and the current gain of β, the differential voltage ΔV_{BE} between two difference size pn junctions is given by:

$$\Delta V_{BE} = V_T \ln N + \frac{I_E}{1+\beta}(r_{b1} - r_{b2}) = \Delta V_{BE,ideal} + \Delta V_{error} \tag{18}$$

Where the emitter current $I_E=I_C+I_B$ is equal to the branch biasing current I_1, and the additional deviation voltage ΔV_{error} caused by base resistance mismatch of $\Delta r_b=r_{b1}-r_{b2}$ is positive due to large r_{b1} under the small base area. So the restriction in determining the CR described by equation (9) will be changed when Δr_b is taken into consideration, which is

$$V_T \ln N = \sqrt{\frac{2I_1}{k_0}}\left(1-\frac{1}{\sqrt{M}}\right) - I_1 \Delta R_{eff} \tag{19}$$

Where the effective ΔR_{eff} can be written as

$$\Delta R_{eff} = \Delta R + \frac{\Delta r_b}{1+\beta} \tag{20}$$

Since $\Delta R_{eff}<0$, as required by (15), the negative ΔR will be altered due to the influence of positive Δr_b, which can be compensated directly by the resistance trimming structure.

Finally, all kind of errors cased by process variation and structure mismatch discussed above are random in nature, meanwhile, all these errors cannot be compensated for each others, and thus the TC degeneration of the CR is serious. This is the reason why the actual TC of CR is far larger than that of the simulation results. So it requires that the resistance trimming should be accurate within a wide dynamic range.

VI. CONCLUSIONS

Completely different to that traditional current summing technique used in current reference generation, the compact temperature compensation methods by suitable combination of ΔV_{BE}, ΔV_{GS} and ΔR are proposed and effectively applied in the current reference circuit. Under optimum mismatch design, the self-biased simplified circuit is convenient for stable current generation. The TC of the output current can be freely configured around zero if the mismatch errors can be reduced and accurately compensated by the trimming techniques.

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